CLAIMS

What is claimed is:

1. An operand file comprising:

at least one pair of future state and architecture state pointers;

an operand queue including at least one entry; and

a reference counter associated with each operand queue entry.

2. The operand file of claim 1, in which a free operand queue entry is assigned to hold a future value of a register of an instruction by writing the free entry's number into the register's future state pointer and incrementing the free entry's reference count.

3. The operand file of claim 2, in which the assigned entry number is written to the register's architectural state pointer and the reference count of the entry previously assigned to the register is decremented upon completion of the instruction.

4. The operand file of claim 3, in which each register is assigned a unique operand queue entry upon a reset.

5. The operand file of claim 3, in which all registers that have undefined value upon reset are assigned to at least one operand queue entry and each of the registers that have defined value upon reset is assigned a unique entry upon a reset.

6. The operand file of claim 3, in which the entry number previously assigned to the register is obtained from the register's future state pointer.

7. The operand file of claim 3, in which the entry number previously assigned to the register is obtained from the register's architectural state pointer.

8. The operand file of claim 3, in which each of the architectural state pointer is copied to its corresponding future state pointer when processing an exception condition.

9. The operand file of claim 3, in which a cancelled instruction does not modify associated architectural state pointers but the reference count of the entry assigned to the register is decremented.

10. The operand file of claim 3, in which a register-copy instruction is executed by copying the operand queue entry number in a source register's future state pointer to a destination register's future state pointer and incrementing the reference count of the associated entry.

11. The operand file of claim 10, in which a register-copy instruction is completed by copying the operand queue entry number in the source register's architectural state pointer to the destination register's architectural state pointer and decrementing the reference count of the entry previously assigned to the destination register.

12. The operand file of claim 10, in which a register-copy instruction is completed by reading the operand queue entry number in the destination register's future state pointer at decode time and writing the entry number to the destination register's architectural state pointer and decrementing the reference count of the entry previously assigned to the destination register.

13. The operand file of claim 10, in which a register-copy instruction copies the future value of the source register to the operand queue entry assigned to the destination register when the reference count of the entry in the source register's future state pointer is at its maximum value.

14. The operand file of claim 10, in which a register-copy instruction copies the future value of the source register to the operand queue entry assigned to the destination register when the reference count of any entry is at its maximum value.

15. The operand file of claim 1, in which an immediate operand is assigned a free operand queue entry by incrementing the reference count of the free entry.

16. The operand file of claim 15, in which the immediate operand is written to the operand queue at any time before the associated instruction needs to read the operand file.

17. The operand file of claim 16, in which the entry assigned to the immediate operand is decremented when the associated instruction is completed.

18. The operand file of claim 16, in which a cancelled instruction with an immediate operand does not modify associated architectural state pointers but the reference count of the entry assigned to hold the immediate operand is decremented.

19. The operand file of claim 16, in which the entry assigned to the immediate operand is decremented as soon as the immediate operand is read.

20. The operand file of claim 3 in which each thread in a multithreaded processor has its own set of architectural and future state pointers but shares one operand queue.

21. The operand file of claim 20 in which all registers that have undefined values in a thread is assigned to at least one free operand queue entry by writing the at least one free entry's number into the thread's architectural and future state pointers and incrementing the at least one entry's reference count by the number of registers.

22. The operand file of claim 20 in which a register in a first thread is copied to a register in a second thread by copying the operand queue entry number in the architectural state pointer of the register in the first thread to the architectural and future state pointers of the register in the second thread and incrementing the reference count of the associated operand queue entry.

23. The operand file of claim 20 in which a register in a first thread is copied to a register in a second thread by copying the operand queue entry number in the future state pointer of the register in the first thread to the architectural and future state pointers of the register in the second thread and incrementing the reference count of the associated operand queue entry.

24. The operand file of claim 20 in which the reference count of the entry in each of a thread's architectural state pointer is decremented by 1 upon terminating the thread.

25. A computer adapted to include an operand file, the operand file comprising:

at least one pair of future state and architecture state pointers;

an operand queue including at least one entry; and

a reference counter associated with each operand queue entry.

26. The computer of claim 25, in which all registers that have undefined value upon reset are assigned to at least one operand queue entry and each of the registers that have defined value upon reset is assigned a unique entry upon a reset.

27. The computer of claim 25, in which each register is assigned a unique operand queue entry upon a reset.

28. The computer of claim 25, in which a free operand queue entry is assigned to hold a future value of a register of an instruction by writing the free entry's number into the

register's future state pointer and incrementing the free entry's reference count.

29. The computer of claim 28, in which the assigned entry number is written to the register's architectural state pointer and the reference count of the entry previously assigned to the register is decremented upon completion of the instruction.